

LM148

Low Power Quad 741 Operational Amplifier

Features

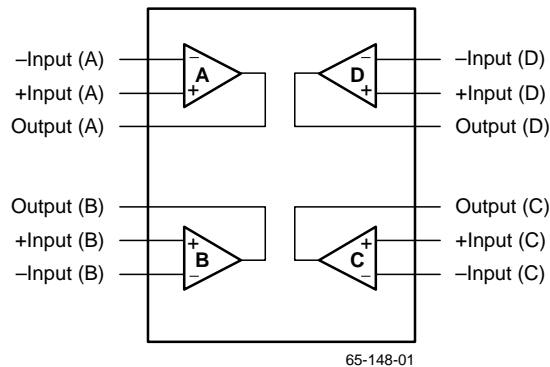
- 741 op amp operating characteristics
- Low supply current drain—0.6 mA/amplifier
- Class AB output stage—no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage—1.0 mV
- Low input offset current—4.0 nA
- Low input bias current—30 nA
- Unity gain bandwidth—1.0 MHz
- Channel Separation—120 dB
- Input and output overload protection

Description

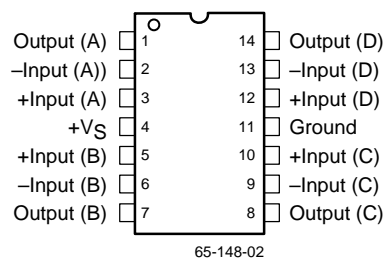
The LM148 is a true quad 741. It consists of four independent high-gain, internally compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias currents which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM148 can be used anywhere multiple 741 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

Block Diagram



Pin Assignments



Absolute Maximum Ratings

| Parameter | Min. | Max. | Unit |
|--------------------------------------------|------------|------|------|
| Supply Voltage | -22 | +22 | V |
| Differential Input Voltage | | 44 | V |
| Input Voltage ¹ | -22 | +22 | V |
| Output Short Circuit Duration ² | Indefinite | | |
| Storage Temperature Range | -65 | +150 | °C |
| Operating Temperature Range | -55 | +125 | °C |
| Lead Soldering Temperature (60 sec.) | +300°C | | |

Notes:

- For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.
- Short circuit to ground on one amplifier only.

Thermal Characteristics

| Parameter | 14-Lead Ceramic DIP |
|----------------------------------------|---------------------|
| Maximum Junction Temperature | +175°C |
| Maximum PD $T_A < 50^\circ\text{C}$ | 1042 mW |
| Thermal Resistance, θ_{JC} | 60°C/W |
| Thermal Resistance, θ_{JA} | 120°C/W |
| For $T_A > 50^\circ\text{C}$ derate at | 8.33 mW/°C |

Electrical Characteristics

($V_S = \pm 15V$ and $T_A = 25^\circ C$, unless otherwise noted)

| Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------|-------------------|----------|----------|------------|
| Input Offset Voltage | $R_S \leq 10K\Omega$ | | 1.0 | 5.0 | mV |
| Input Offset Current | | | 4.0 | 25 | nA |
| Input Bias Current | | | 30 | 100 | nA |
| Input Resistance (Differential Mode) ¹ | | 0.8 | 2.5 | | M Ω |
| Supply Current, All Amplifiers | $V_S = \pm 15V$ | | 2.4 | 3.6 | mA |
| Large Signal Voltage Gain | $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2K\Omega$ | 50 | 160 | | V/mV |
| Channel Separation | $F = 1 \text{ Hz } 20 \text{ KHz}$ | | 120 | | dB |
| Unity Gain Bandwidth | | | 1.0 | | MHz |
| Phase Margin | | | | 60 | Degrees |
| Slew Rate | | | | 0.5 | V/ μ S |
| Short Circuit Current | | | 25 | | mA |
| The following specifications apply for $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$. | | | | | |
| Input Offset Voltage | $R_S \leq 10K\Omega$ | | | 6.0 | mV |
| Input Offset Current | | | | 75 | nA |
| Input Bias Current | | | | 325 | nA |
| Large Signal Voltage Gain | $V_S = \pm 15V$, $V_{OUT} = 10V$, $R_L < 2K\Omega$ | 25 | | | V/mV |
| Output Voltage Swing | $V_S = \pm 15V$ | $R_L = 10K\Omega$ | ± 12 | ± 13 | V |
| | | $R_L = 2K\Omega$ | ± 10 | ± 12 | |
| Input Voltage Range | $V_S = \pm 15V$ | ± 12 | | | V |
| Common Mode Rejection Ratio | $R_S \leq 10K\Omega$ | 70 | 90 | | dB |
| Power Supply Rejection Ratio | $R_S \leq 10K\Omega$ | 77 | 96 | | dB |

Note:

1. Guaranteed by design but not tested.

Typical Performance Characteristics

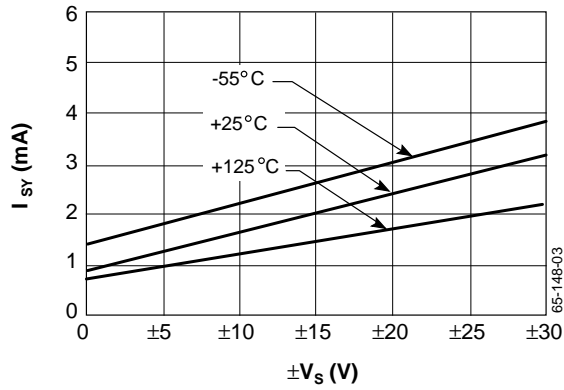


Figure 1. Supply Current vs. Supply Voltage

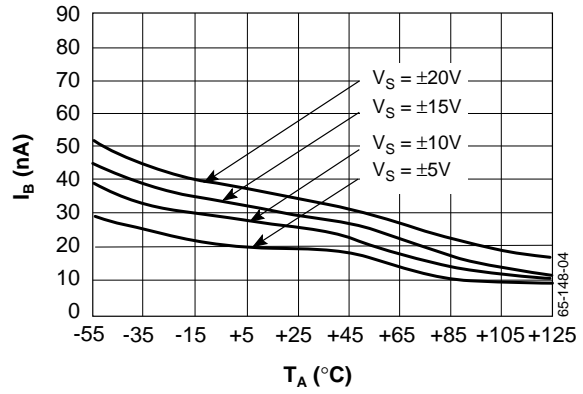


Figure 2. Input Bias Current vs. Temperature

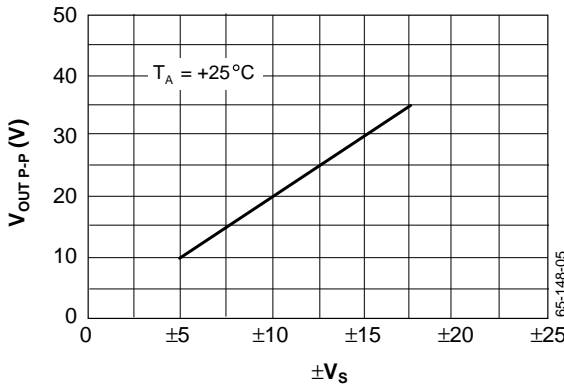


Figure 3. Output Voltage Swing vs. Supply Voltage

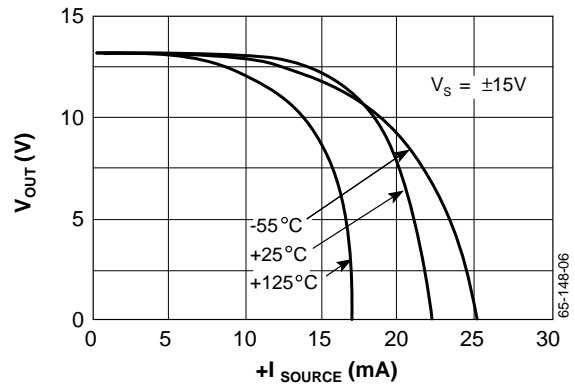


Figure 4. Positive Current Limit Output Voltage vs. Output Source Current

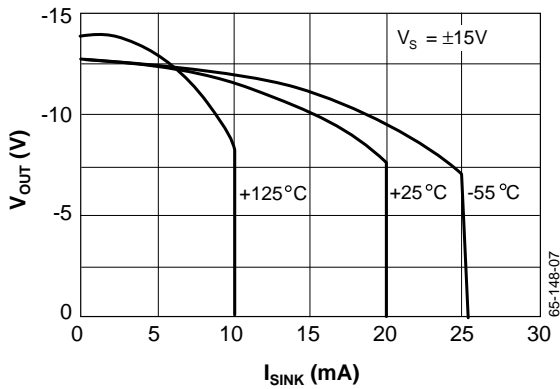


Figure 5. Negative Current Limit Output Voltage vs. Output Sink Current

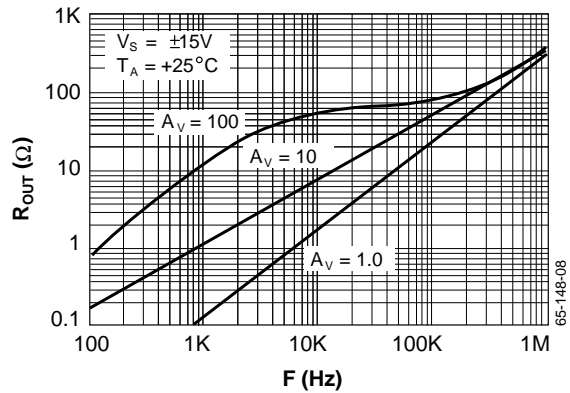


Figure 6. Output Impedance vs. Frequency

Typical Performance Characteristics (continued)

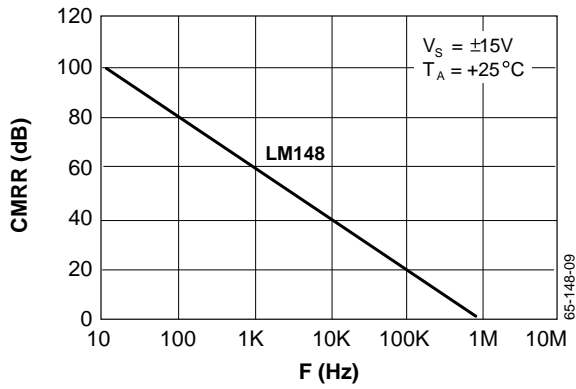


Figure 7. CMRR vs. Frequency

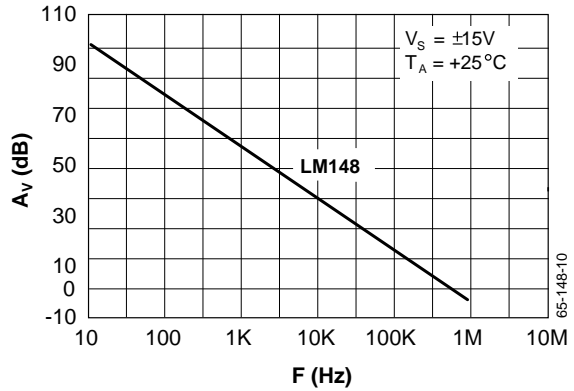


Figure 8. Open Loop Gain vs. Frequency

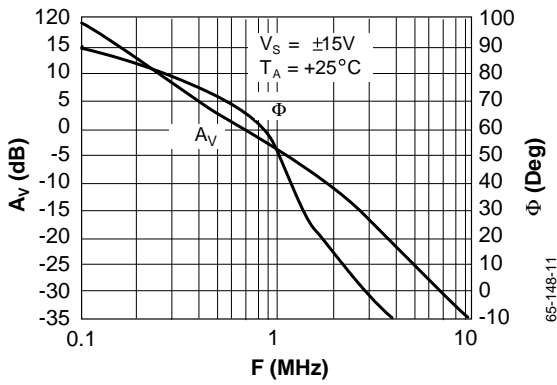


Figure 9. Gain, Phase vs. Frequency

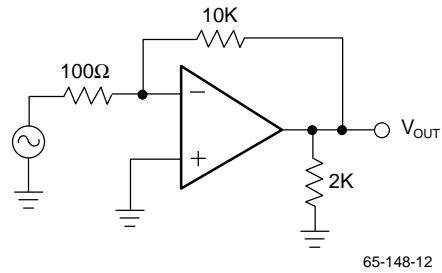


Figure 10. Gain, Phase Test Circuit

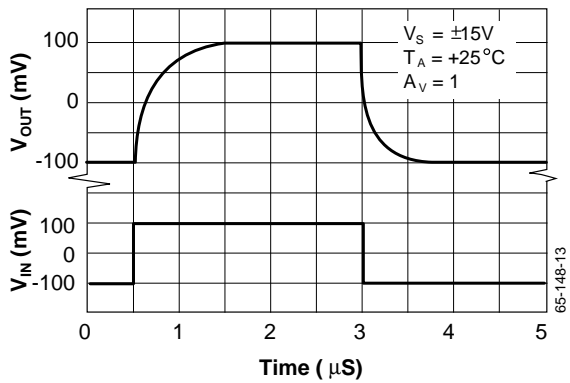


Figure 11. Small Signal Pulse Response Input, Output Voltage vs. Time

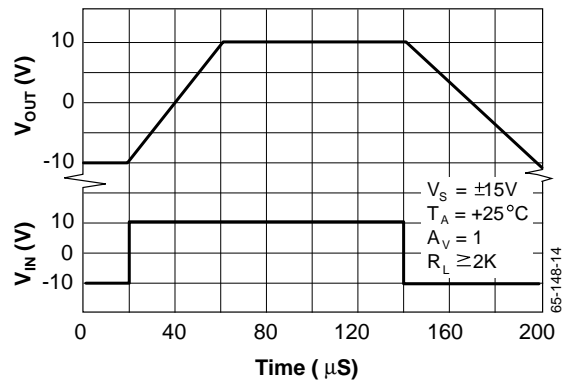


Figure 12. Large Signal Pulse Response Output Voltage vs. Time

Typical Performance Characteristics (continued)

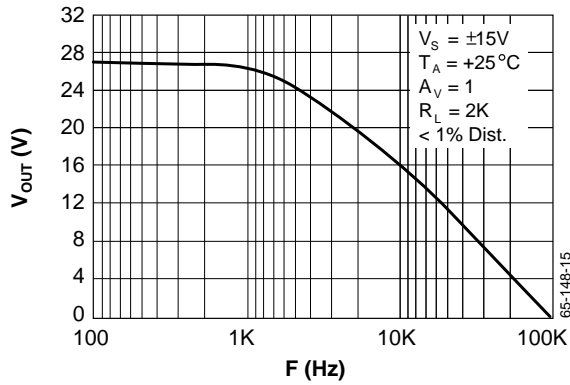


Figure 13. Undistorted Output Voltage Swing vs. Frequency

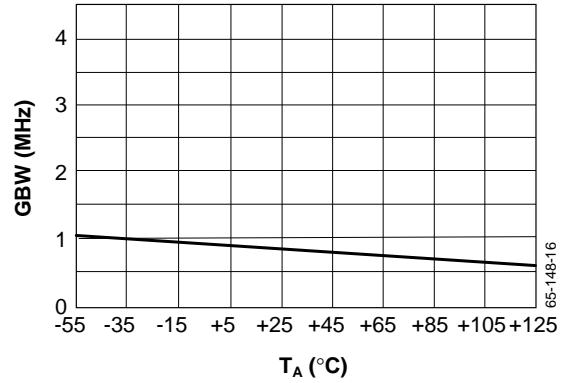


Figure 14. Gain Bandwidth Product vs. Temperature

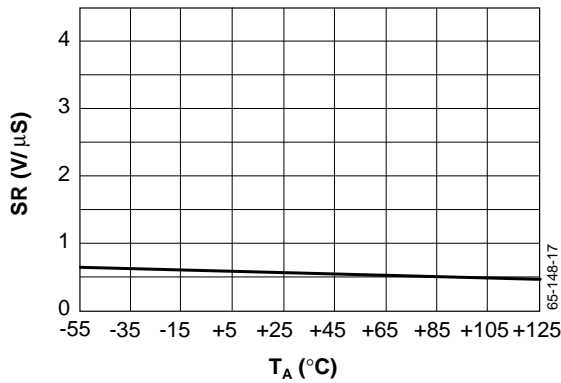


Figure 15. Slew Rate vs. Temperature

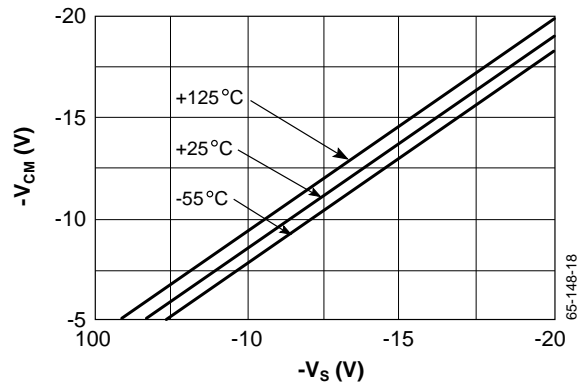


Figure 16. Negative Common Mode Input Voltage vs. Supply Voltage

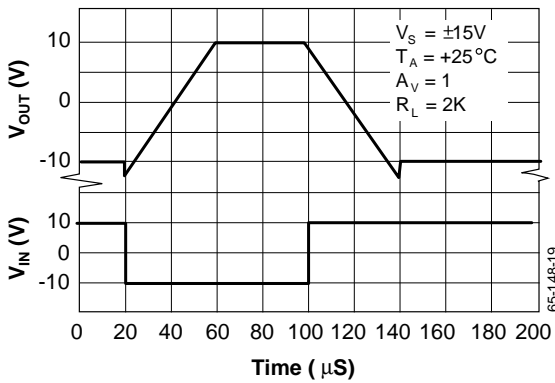


Figure 17. Inverting Large Signal Pulse Response Input, Output Voltage vs. Time

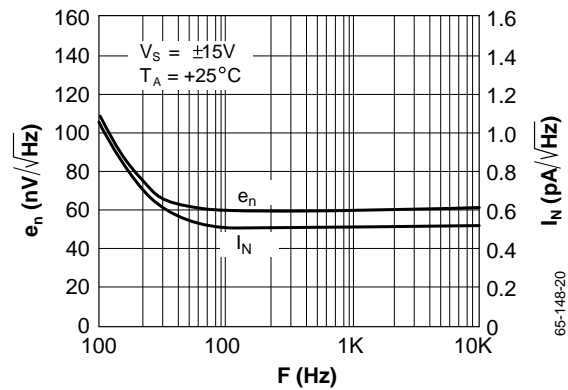


Figure 18. Input Noise Voltage, Current Densities vs. Frequency

Typical Performance Characteristics (continued)

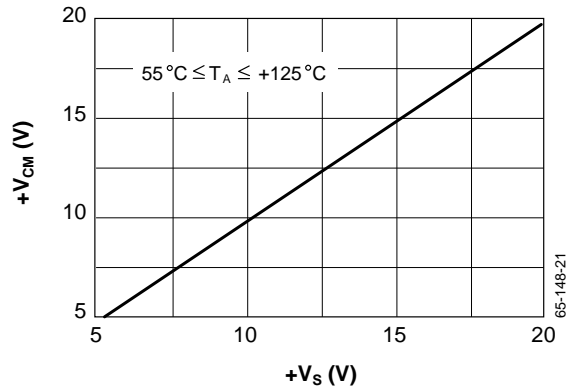


Figure 19. Positive Common Mode, Input Voltage vs. Supply Voltage

Typical Simulation

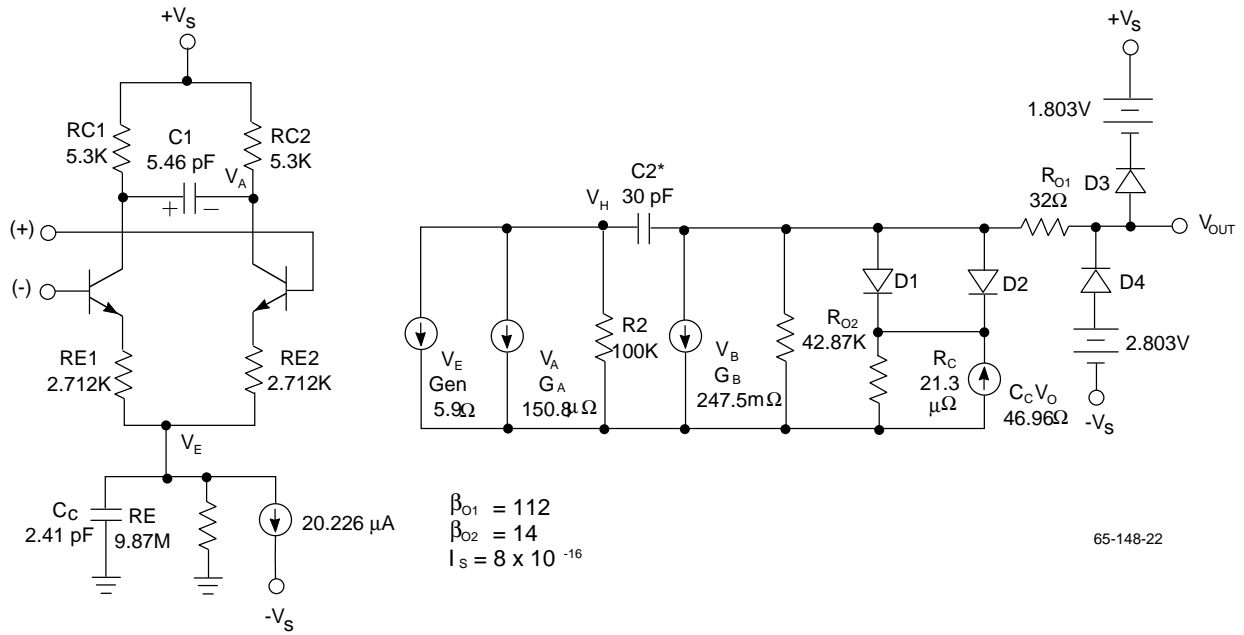


Figure 20. LM148 Macromodel for Computer Simulation

Applications Discussion

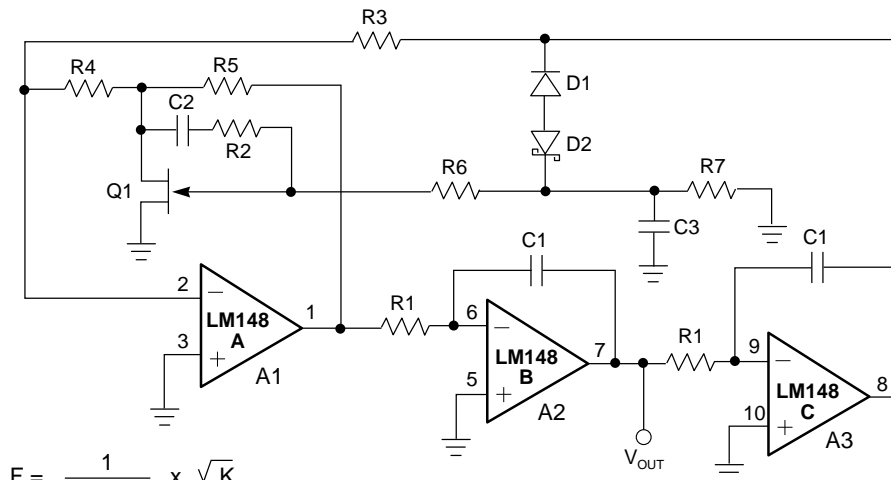
The LM148 low power quad operational amplifier exhibits performance comparable to the popular 741. Substitution can therefore be made with no change in circuit behavior.

The input characteristics of these devices allow differential voltages which exceed the supplies. Output phase will be correct as long as one of the inputs is within the operating common mode range. If both exceed the negative limit, the output will latch positive. Current limiting resistors should be used on the inputs in case voltages become excessive.

When capacitive loading becomes much greater than 100pF, a resistor should be placed between the output and feedback connection in order to reduce phase shift.

The LM148 is short circuit protected to ground and supplies continuously when only one of the four amplifiers is shorted. If multiple shorts occur simultaneously, the unit can be destroyed due to excessive power dissipation.

To assure stability and to minimize pickup, feedback resistors should be placed close to the input to maximize the feedback pole frequency (a function of input to ground capacitance). A good rule of thumb is that the feedback pole frequency should be 6 times the operating -3.0B frequency. If less, a lead capacitor should be placed between the output and input.



$$F = \frac{1}{2\pi R_1 C_1} \times \sqrt{K}$$

$$K = \frac{R_4 R_5}{R_3} \left(\frac{1}{R_{DS}} + \frac{1}{R_4} + \frac{1}{R_5} \right)$$

$$R_{DS} \cong \left(\frac{R_{ON}}{1 - \frac{V_{GS}}{V_P}} \right)^{1/2}$$

$$F_{MAX} = 5.0 \text{ KHz}, \text{ THD} \leq 0.03\%$$

$$R_1 = 100\text{K pot.}, C_1 = 0.0047 \mu\text{F}, C_2 = 0.01 \mu\text{F}, C_3 = 0.1 \mu\text{F}, R_2 = R_6 = R_7 = 1\text{M}, R_3 = 5.1\text{K}, R_4 = 12\Omega.$$

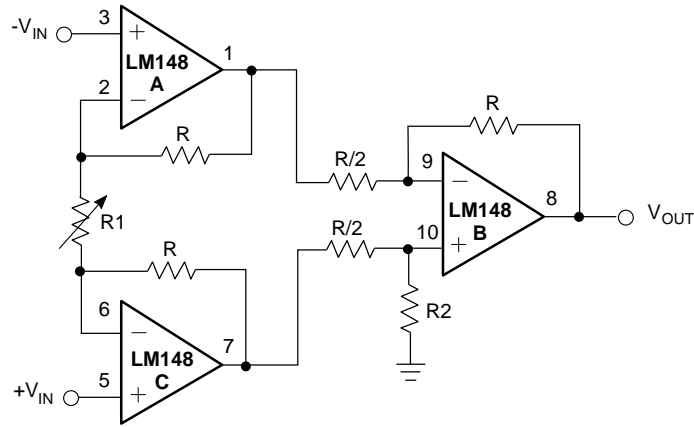
$$R_5 = 240\Omega, Q_1 = \text{NS5102}, D_1 = 1\text{N914}, D_2 = 3.6\text{V avalanche diode (ex. LM103)}, V_S = \pm 15\text{V}$$

A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in feedback loop of A3.

65-148-23

Figure 21. One Decade Low Distortion Sinewave Generator

Applications Discussion (continued)



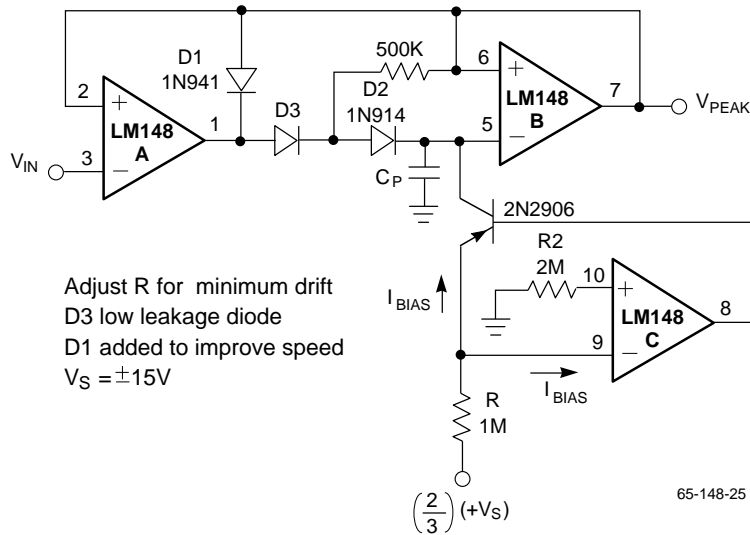
$$V_{OUT} = 2 \left(\frac{2R}{R1} + 1 \right) \cdot (-V_S - 3V) \leq V_{IN CM} \leq (+V_S - 3V)$$

$$V_S = \pm 15V$$

R = R2, trim R2 to boost CMRR

65-148-24

Figure 22. Low Cost Instrumentation Amplifier



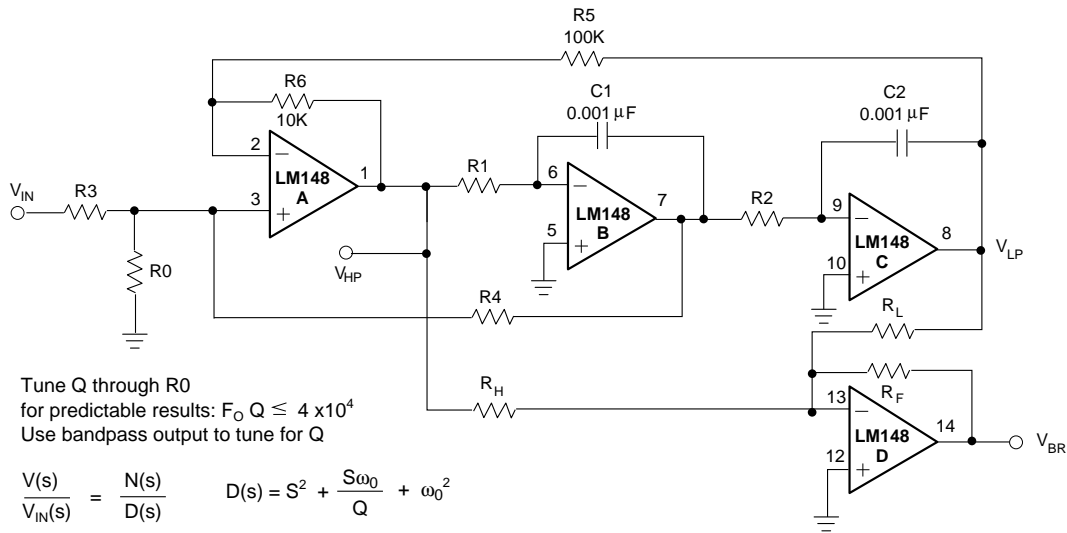
Adjust R for minimum drift
 D3 low leakage diode
 D1 added to improve speed
 $V_S = \pm 15V$

$$\left(\frac{2}{3} \right) (+V_S)$$

65-148-25

Figure 23. Low Voltage Peak Detector with Bias Current Compensation

Applications Discussion (continued)



Tune Q through R_0
 for predictable results: $F_0 Q \leq 4 \times 10^4$
 Use bandpass output to tune for Q

$$\frac{V(s)}{V_{IN}(s)} = \frac{N(s)}{D(s)} \quad D(s) = S^2 + \frac{S\omega_0}{Q} + \omega_0^2$$

$$N_{HP}(s) = S^2 H_{OHP}, \quad N_{BP}(s) = \frac{-S\omega_0 H_{OBP}}{Q} \quad N_{LP} = \omega_0^2 H_{OLP}$$

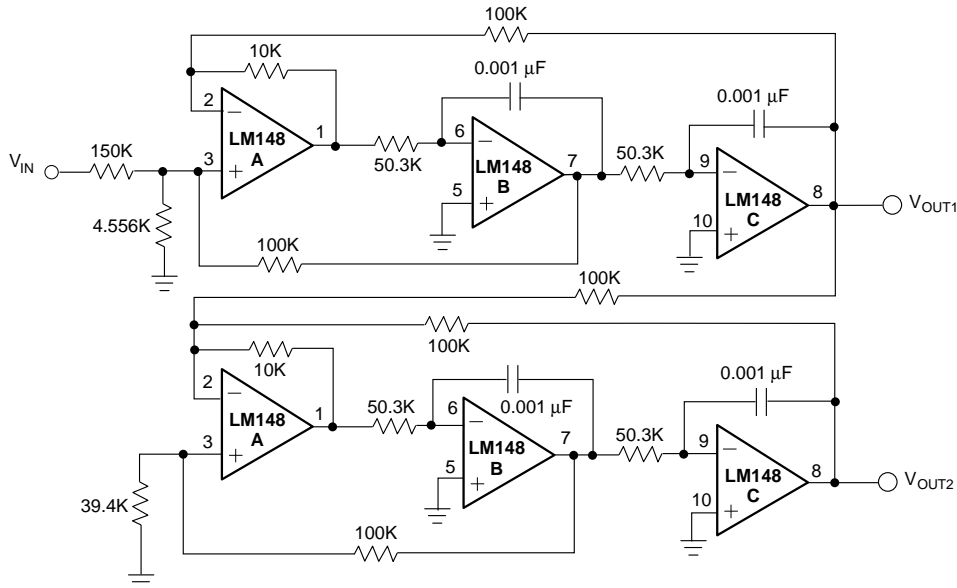
$$F_0 = \frac{1}{2\pi} \sqrt{\frac{R_6}{R_5}} \sqrt{\frac{1}{t_1 t_2}}, \quad t_1 = R_1 C_1, \quad Q = \left(\frac{1 + R_4 | R_3 + R_4 | R_0}{1 + R_6 | R_5} \right) \left(\frac{R_6}{R_5} \frac{t_1}{t_2} \right)^{1/2}$$

$$F_{NOTCH} = \frac{1}{2\pi} \left(\frac{R_H}{R_L t_1 t_2} \right)^{1/2}, \quad H_{OHP} = \frac{1 + R_6 | R_5}{1 + R_3 | R_0 + R_3 | R_4}, \quad H_{OBP} = \frac{1 + R_4 | R_3 + R_4 | R_0}{1 + R_3 | R_0 + R_3 | R_4}$$

$$H_{OLP} = \frac{1 + R_5 | R_6}{1 + R_3 | R_0 + R_3 | R_4}$$

65-148-26

Figure 24. Universal State-Space Filter

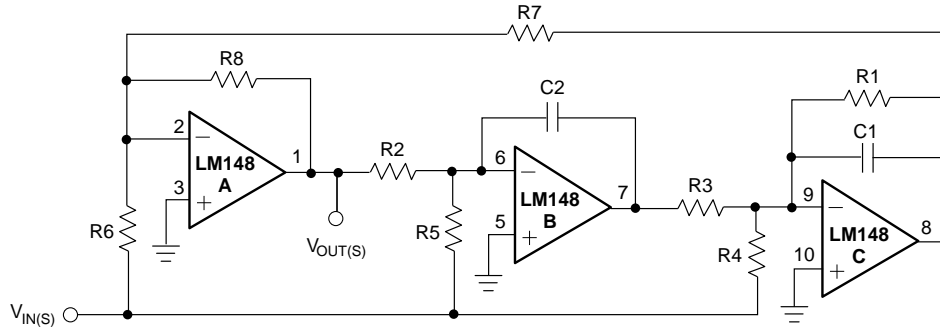


Use general equations, and tune each section separately.
 Q_{1st} Section = 0.541, Q_{2nd} Section = 1.306.
 The response should have 0 dB peaking.

65-148-27

Figure 25. 1 KHz 4-Pole Butterworth Filter

Applications Discussion (continued)



$$Q = \sqrt{\frac{R8}{R7}} \left(\frac{R1C1}{\sqrt{R3C2R2C1}} \right), F_o = \frac{1}{2\pi} \sqrt{\frac{R8}{R7}} \left(\frac{1}{\sqrt{R2R3C1C2}} \right), F_{NOTCH} = \frac{1}{2\pi} \sqrt{\frac{R6}{R3R5R7C1C2}}$$

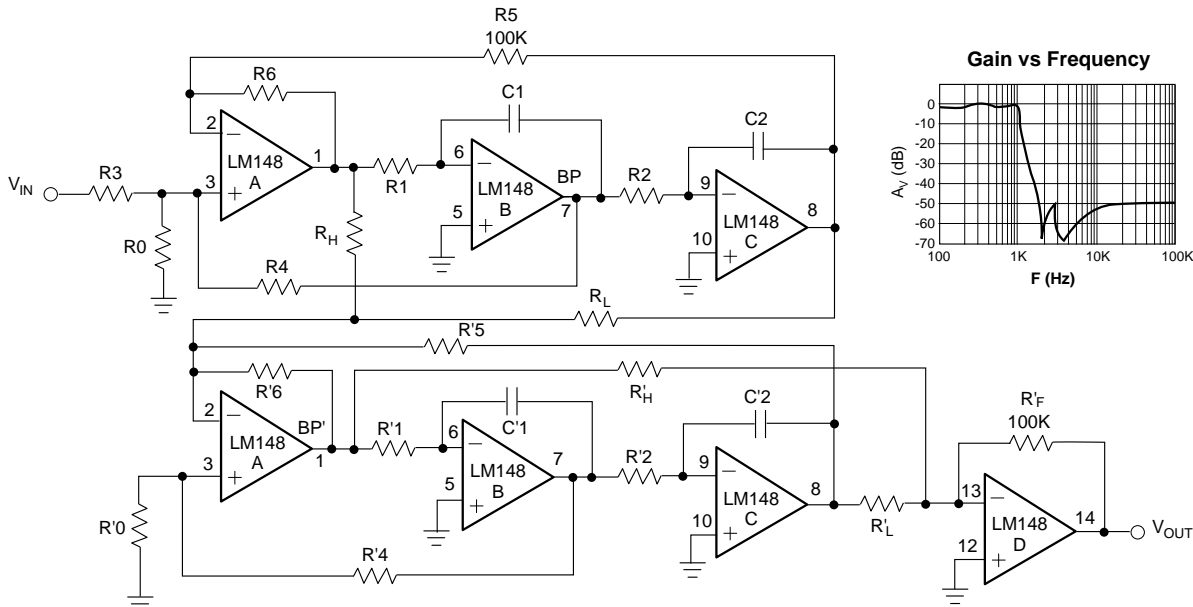
Necessary condition for notch : $\frac{1}{R6} = \frac{R1}{R4R7}$

Examples: $F_{NOTCH} = 3 \text{ kHz}$, $Q = 5$, $R1 = 270\text{K}$, $R2 = R3 = 20\text{K}$, $R4 = 27\text{K}$, $R5 = 20\text{K}$, $R6 = R8 = 10\text{K}$, $R7 = 100\text{K}$.
 $C1 = C2 = 0.001 \mu\text{F}$.

Better noise performance than the state-space approach.

65-148-28

Figure 26. 3 Amplifier Bi-Quad Notch Filter



$F_C = 1 \text{ kHz}$, $F_S = 2 \text{ kHz}$, $F_P = 0.543$, $F_Z = 2.14$, $Q = 0.841$, $F'_P = 0.987$, $F'_Z = 4.92$.
 $Q' = 4.403$ normalized to ripple BW.

$$F_P = \frac{1}{2\pi} \sqrt{\frac{R6}{R5}} \left(\frac{1}{t} \right), F_Z = \frac{1}{2\pi} \sqrt{\frac{R_H}{R_L}} \left(\frac{1}{t} \right), Q = \frac{1 + R4/R3 + R4/R0}{1 + R6/R5} \times \sqrt{\frac{R6}{R5}}, Q' = \sqrt{\frac{R6}{R5}} \times \frac{1 + R4/R0}{1 + R6/R5 + R6/R_P}$$

$$R_P = \frac{R_H R_L}{R_H + R_L}$$

Use the B/P outputs to tune Q, Q', tune the 2 sections separately.

$R1 = R2 = 92.6\text{K}$, $R3 = R4 = R5 = 100\text{K}$, $R6 = 10\text{K}$, $R0 = 107.8\text{K}$, $R_L = 100\text{K}$, $R_H = 155.1\text{K}$,
 $R'1 = R'2 = 50.9\text{K}$, $R'4 = R'5 = 100\text{K}$, $R'6 = 10\text{K}$, $R'0 = 5.78\text{K}$, $R'_L = 100\text{K}$, $R'_H = 248.12\text{K}$, $R'_F = 100\text{K}$.

65-148-29

All capacitors are $0.001 \mu\text{F}$.

Figure 27. 4th Order 1 KHz Elliptic Filter (4 Poles, 4 Zeros)

Notes:

Notes:

Notes:

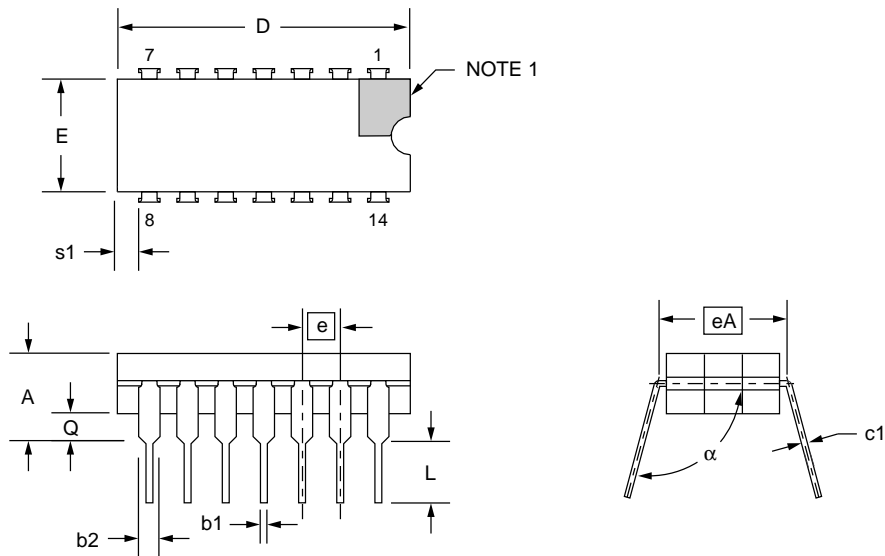
Mechanical Dimensions

14-Pin Ceramic DIP

| Symbol | Inches | | Millimeters | | Notes |
|----------|----------|------|-------------|-------|-------|
| | Min. | Max. | Min. | Max. | |
| A | — | .200 | — | 5.08 | |
| b1 | .014 | .023 | .36 | .58 | 8 |
| b2 | .045 | .065 | 1.14 | 1.65 | 2 |
| c1 | .008 | .015 | .20 | .38 | 8 |
| D | — | .785 | — | 19.94 | 4 |
| E | .220 | .310 | 5.59 | 7.87 | 4 |
| e | .100 BSC | | 2.54 BSC | | 5, 9 |
| eA | .300 BSC | | 7.62 BSC | | 7 |
| L | .125 | .200 | 3.18 | 5.08 | |
| Q | .015 | .060 | .38 | 1.52 | 3 |
| s1 | .005 | — | .13 | — | 6 |
| α | 90° | 105° | 90° | 105° | |

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within $\pm .010$ (.25mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (leads number 1, 7, 8, and 14).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when " α " is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twelve spaces.



Ordering Information

| Part Number | Package | Operating Temperature Range |
|-------------|---------------------|-----------------------------|
| LM148D | 14-Lead Ceramic DIP | -55°C to +125°C |
| LM148D/883B | 14-Lead Ceramic DIP | -55°C to +125°C |

Note:

1. 883B suffix denotes Mil-Std-883, Level B processing

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